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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,176	03/05/2002	Charles Patton	5181-84600	9947

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EXAMINER	
HARRISON, CHANTE E	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 11/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,176	PATTON, CHARLES	
	Examiner	Art Unit	
	Chante Harrison	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/15/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the following communication: Request for Reconsideration filed on 9/15/06. This action is made FINAL.

2. Claims 18-40 are pending in this application. Claims 18, 26 and 34 are independent claims.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 18-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masaki Takeda, US 5,559,937, 9/1996 and further in view of Debra Kipping, US 6,831,660 B1, 12/2004.

As per independent claim 18, Takeda discloses passing the pixel location through a plurality of clip circuits (i.e. passing polygon vertex data, col. 8, ll. 39-44; col. 20, ll. 59-65, through clip circuits Fig. 6C "420 a & b"), wherein the clip circuits are connected in series to form a pipeline (Fig. 6c "420 a & b" connected in series col. 11, ll. 30-35), and wherein each clip circuit is a segment of the pipeline (Fig. 6c "420 a & b" are segments of pipeline "410"); computing a window result (i.e. inside/outside decision stored as specification data) in each clip circuit for the pixel location (i.e. an inside/outside decision, col. 18, ll. 50-55, is performed on each vertex coordinate, col. 20, ll. 65-67, and is fed through the pipeline, col. 11, ll. 20-35; col. 20,ll. 7-27; Fig. 6), wherein each clip circuit is provided data defining a different display region (Fig. 6c; col. 11, ll. 25-40; col. 15, ll. 4-10), wherein the window result comprises an indication of inclusion of the pixel location within the corresponding display region (col. 18, ll. 52-56); outputting the

pixel location and a window word from each clip circuit (col. 20-21, ll. 65-32), wherein said outputting comprises, passing the pixel location and the window word directly to a next clip circuit in the series of clip circuits (Fig. 6c; col. 21, ll. 25-30; col. 22, ll. 25-32) except for the last clip circuit in the series (col. 22, ll. 32-35), and wherein the window word also comprises any previous window results (i.e. the inside/outside decision results are used as input to the next clip circuit when further polygon vertex processing is required) (col. 11, ll. 20-35; Fig. 6c; col. 22,ll. 25-30), and examining the window word output by the last clip circuit in the series of clip circuits to determine if the pixel is included in at least one of the display regions (col. 20-21, ll. 65-32).

Takeda fails to disclose a plurality of windows.

Kipping discloses a plurality of windows (Fig. 5 "500, 502") processed by clip circuits that execute sequentially in a pipeline (Fig. 3 "320"; col. 1, ll. 45-55) to determine display data inclusion within a window (abstract).

It would have been obvious to one of skill in the art to include in the method of Takeda a plurality of windows as taught by Kipping because Takeda teaches applying a serial clipping pipeline to determine polygon vertex inclusion or exclusion within a display region, a boundary region and an out of display region, where each region is a two dimensional space defined by coordinates. Defining various display regions by 2D coordinates provides the advantage of determining in which display area or window polygon data does or does not exist, so that only desired data is processed, which increases display processing speed.

As per dependent claims 19 and 27, Takeda discloses said pixel location comprises a horizontal and a vertical coordinate that define position of said pixel on a screen (col. 8, ll. 39-44; col. 10, ll. 50-60).

As per dependent claims 20, 28 and 35, Takeda discloses a 2D display region (Fig. 19 "20"; col. 13, ll. 1-7) for displaying data defined by screen coordinates, x and y, (col. 10, ll. 50-55).

Takeda fails to disclose each of the plurality of windows comprises a first horizontal and a second horizontal coordinate and a first vertical and a second vertical coordinate that define each window's boundaries on the screen.

Kipping discloses a plurality of windows comprising respective first and second horizontal and vertical coordinates (col. 4, ll. 60-66; col. 7, ll. 35-40).

It would have been obvious to one of skill in the art to include in the method of Takeda a window comprising respective first and second horizontal and vertical coordinates as taught by Kipping because a window is a display region. Defining a window or display region by respective first and second horizontal and vertical coordinates provides the benefit of creating respective upper, lower and side edges that define a boundary to determine inclusion or exclusion of displayed data with respect to the display region or window. Additionally, it would have been obvious to one of skill in the art to include Kipping's plurality of windows with the method of Takeda. The rationale as applied in the above rejection of claims 18, 26 and 34 applies herein.

As per dependent claims 21 and 29, Takeda discloses wherein said computing window result computing horizontal inclusion by computing if said horizontal pixel coordinate is located between the first horizontal and the second horizontal coordinate of the corresponding window (i.e. inside/outside decision processing the polygon vertex coordinates to determine inclusion within zone defining display region "20", Fig. 19) (col. 15, ll. 4-10; col. 18, ll. 43-55), and computing vertical inclusion if said vertical pixel coordinate is located between the first vertical and the second vertical coordinate of the corresponding window (i.e. inside/outside decision processing the polygon vertex coordinates to determine inclusion within zone defining display region "20", Fig. 19) (col. 15, ll. 4-10; col. 18, ll. 43-55).

As per dependent claims 22 and 30, Takeda discloses wherein said computing window result further comprises: setting the indication of inclusion of the pixel to positive if both the horizontal and vertical inclusions are true (i.e. setting specification to output the data) (col. 21, ll. 20-24), and setting the indication of inclusion to negative if one or more of the horizontal and vertical inclusions are false (i.e. setting a specification to ignore the polygon vertex data) (col. 21, ll. 14-19).

As per dependent claims 23, 31 and 36, Takeda discloses clipping the pixel if said examining determines that the pixel is not included in the display region (col. 10, ll. 38-50), and propagating the pixel if said examining determines that the pixel is included in at least one window (col. 10, ll. 38-50).

Takeda fails to disclose a plurality of windows, which Kipping discloses (Fig. 5 "500 & 502").

The rationale as applied in the rejection of claims 18, 27 and 34 applies herein. As per dependent claims 24, 32 and 37, Takeda discloses a 2D display region, and an out of display region (Fig. 19 "20"; col. 13, ll. 1-7).

Takeda fails to discloses wherein said plurality of windows comprise two or more 2-D windows, which Kipping discloses (col. 6, ll. 1-5).

It would have been obvious to one of skill in the art to include in the method of Takeda two or more 2D windows as taught by Kipping because Takeda teaches applying a serial clipping pipeline to determine polygon vertex inclusion or exclusion within a display region and an out of display region, where each region is a two dimensional space defined by coordinates. Defining various display regions by 2D coordinates provides the advantage of determining in which display area or window polygon data does or does not exist, so that only desired data is processed, which increases display processing speed.

As per dependent claims 25, 33 and 38, Takeda discloses said plurality of clip circuits (Fig. 6c; col. 11, ll. 25-40).

Takeda fails to disclose the circuits are identical.

It would have been obvious to one of skill in the art to include identical circuits with the method of Takeda because Takeda teaches a single clip circuit for performing polygon processing using an internal loop to process data multiple times for different

display regions. Takeda also teaches a plurality of clip circuits in series for performing the same polygon processing by passing data through the pipeline. Therefore, the plurality of clip circuits, which perform the same processing, as a single clip circuit using an internal loop, are identical. Using identical clip circuits provides the advantage of increased speed of clip processing.

As per independent claim 26, Kipping discloses supplying window boundary coordinates for a display region to each clip circuit (col. 9, ll. 21-25) of a plurality of clip circuits (Fig. 6c "420") connected in a series (Fig. 6c; col. 11, 30-35), determining inclusion of a pixel in the corresponding display region in each clip circuit (col. 20-21, ll. 65-32).

Takeda fails to disclose a plurality of windows.

The rationale as applied in the rejection of independent claim 18 applies herein.

As per independent claim 34, Takeda discloses a plurality of clip circuits connected in a series (Fig. 6c "420a & b"), wherein each circuit in the series is configured to: (a) receive horizontal and vertical coordinates locating a pixel (i.e. vertex coordinates are supplied to the clipping calculation section "200", Fig. 15) (col. 20, ll. 45-65), (b) receive horizontal and vertical coordinates defining a display region (col. 9, ll. 21-25), (c) compute a window result indicating inclusion of the pixel within the corresponding window defined in (b) (col. 20-21, ll. 65-32).

As per dependent claim 39, Takeda discloses each clip circuit of the plurality of clip circuits is directly connect to the next clip circuit in the series of clip circuits (Fig. 6c).

As per dependent claim 40, Takeda discloses the plurality of clip circuits form a pipeline (col. 11, ll. 32-35), and each clip circuit is a segment of the pipeline (Fig. 6c).

Response to Arguments

3. Applicant's arguments filed 9/15/06 have been fully considered but they are not persuasive. Applicant argues Kipping and Takeda either singly or in combination do not teach "computing a window result in each clip circuit for the pixel location, wherein each clip circuit is provided data defining one of the plurality of window, wherein the window result comprises an indication of inclusion of the pixel location within the corresponding one of the plurality of windows".

In response, Takeda teaches performing clipping processing using two clipping processing devices "420a" and "420b". Thus, each of the clipping processing devices corresponds to a clipping circuits. Takeda teaches clipping processing devices "420a" and "420b" processes respective surfaces having object/polygon data in designated zones of the display region comprising a window (col. 11, ll. 25-40; col. 15, ll. 4-10). Thus, Takeda teaches the clip circuits being provided data for a window for processing. Takeda teaches an inside/outside decision, col. 18, ll. 50-55, is performed on each vertex coordinate, col. 20, ll. 65-67, and is fed through the pipeline, col. 11, ll. 20-35; col. 20,ll. 7-27; Fig. 6. Thus, the determination of polygon/pixel data being designated as either inside or outside, corresponds to computing a window result that determines inclusion of the polygon/pixel.

Applicant argues Takeda does not teach outputting a pixel location and window word from each clip circuit comprising passing the pixel through clip circuits connected in a series to form a pipeline.

In response, Takeda specifically teaches the clip processing devices are connected in series and perform pipeline processing (Fig. 6C; col. 11, ll. 30-35). Additionally, Takeda teaches an internal loop is formed between the plurality of clipping processing devices such that the input is connected to the output which results in data for the next clipping processing to be performed using data from the first clipping processing (col. 11, ll. 4-11). Thus, Takeda teaches passing the pixel through clip circuits connected in a series to form a pipeline. Takeda also teaches clipping processing calculating vertex coordinates, e.g. pixel location, col. 20-21, ll. 65-32 and performing an inside/outside decision, col. 18, ll. 50-55, on each vertex coordinate, col. 20, ll. 65-67, and feeding the decision through the pipeline, col. 11, ll. 20-35; col. 20,ll. 7-27; Fig. 6. Thus, Takeda teaches outputting a pixel location and window word from each clip circuit comprising passing the pixel through clip circuits connected in a series to form a pipeline.

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chante Harrison whose telephone number is 571-272-7659. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Chante Harrison
Examiner
Art Unit 2628

Ch
November 20, 2006

KEE M. TUNG
SUPERVISORY PATENT EXAMINER